REMARKS

Applicants thank the Examiner for the thorough consideration given the present application.

Claims 1-9 are pending in the application. Claims 1 and 5 are independent. Claims 1, 5 and 7 have been amended.

The following remarks are believed to be fully responsive to the Office Action, and to render all the claims at issue patentably distinguishable over the cited references. Reconsideration of this application, as amended, is respectfully requested.

Claim Rejections Under 35 U.S.C. § 112, 2nd Paragraph

Claim 7 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. It is respectfully submitted that amended claim 7 is clear, definite, and provides full support for the elements recited therein. Accordingly, withdrawal of the rejection of claim 7 under 35 U.S.C. § 112, second paragraph, is respectfully requested.

Claim Rejections Under 35 U.S.C. §§ 102(b) and 103(a)

Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,547,888 to Yamazaki. Claims 4 and 7-9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki. Claim 3 is rejected under 35 U.SC. §103(a) as being unpatentable over Yamazaki in

view of U.S. Patent No. 5,602,410 to Schwalke et al. These rejections are respectfully traversed.

While not conceding the appropriateness of the rejections, but merely to expedite the prosecution of the instant application, independent claim 1 is amended to recite a combination of elements in a semiconductor device including "sidewall spacers, each sidewall spacer being formed to abut against both a side of the first or second conductor structures and a side of the insulator structure such that a vertical portion of each sidewall spacer abuts the conductor structures, the sidewall spacers manifesting the self-aligned contact hole in the region between the first and second conductor structures, wherein the self-aligned contact hole does not overlap any part of the first and second conductor structures."

Similarly, independent claim 5 is amended to recite a combination of elements in an unsymmetrical semiconductor device, including "first sidewall spacers, each first sidewall spacer being formed to abut against both a side of the first or second conductor structures and a side of an insulator structure such that a vertical portion of each sidewall spacer abuts the conductor structures, the first sidewall spacers manifesting the self-aligned contact hole in the region between the first and second conductor structures, wherein the self-aligned contact hole does not overlap any part of the first and second conductor structures."

It is respectfully submitted that the combinations of elements recited in claims 1 and 5, as amended, are not disclosed or made obvious over the applied prior art of record, including Yamazaki and Schwalke et al.

Yamazaki discloses a method of manufacturing an unsymmetrical semiconductor device which includes two gate electrodes 4, a sidewall silicon layer 6D and contact holes 9D and 9S formed in an insulating layer in order to expose parts of the two gate electrodes 4, as shown, for example, in Figs. 10 and 11. The semiconductor device structure taught in Yamazaki is very different from that of the present invention, however, which is directed to an unsymmetrical semiconductor device using a self-aligned contact hole, which does not expose any part of a first and second gate electrodes.

Yamazaki does not teach or suggest "sidewall spacers, each sidewall spacer being formed to abut against both a side of the first or second conductor structures and a side of the insulator structure such that a vertical portion of each sidewall spacer abuts the conductor structures, the sidewall spacers manifesting the self-aligned contact hole in the region between the first and second conductor structures, wherein the self-aligned contact hole does not overlap any part of the first and second conductor structures," as recited in claim 1.

Moreover, Yamazaki does not teach or suggest "first sidewall spacers, each first sidewall spacer being formed to abut against both a side of the first

or second conductor structures and a side of an insulator structure such that a vertical portion of each sidewall spacer abuts the conductor structures, the first sidewall spacers manifesting the self-aligned contact hole in the region between the first and second conductor structures, wherein the self-aligned contact hole does not overlap any part of the first and second conductor structures," as recited in claim 5.

At least for the reasons that the independent claims 1 and 5 are allowable, the dependent claims 2 and 6 depending thereupon include the patentable features of claims 1 and 5.

In rejecting claims 4 and 7-9, the Office Action relies further on Yamazaki for the teachings in these claims. However, the Office Action goes on to concede that Yamazaki does not actually teach the limitations of claims 4 and 7-9, but that these claim limitations would have been obvious to one having ordinary skill in the art. Applicants respectfully disagree with this contention and respectfully submit that Yamazaki does not teach or suggest "the contact structure is a plug" as recited by claims 4 and 7, "a device, wherein the plug is in contact with a bit line" as recited in claim 8 and "a device, wherein the contact plug is not disposed directly above the first and second conduct structures" as recited in claim 9. Applicants respectfully request the Examiner to produce one or more references that teach each of the limitations of claims 4 and 7-9. M.P.E.P. § 2143 states that "the prior art

reference (or references when combined) must teach or suggest all the claim limitations." Accordingly, until such references are produced, the rejections of claims 4 and 7-9 under 35 U.S.C. §103(a) based on Yamazaki are deemed improper.

In rejecting claim 3, the Office Action relies on Schwalke et al. for a teaching of a gate including a cap insulating layer. Schwalke et al. discloses a method of manufacturing a flash EEPROM cell with a split-gate structure. However, Schwalke et al. does not teach or suggest the above-cited limitations of claim 1, and therefore does not cure the deficiencies of Yamazaki with respect to claim 1, as incorporated in claim 3. Moreover, Schwalke et al. does not each or suggest the above-cited limitations of claim 5.

In view of the foregoing, it is respectfully submitted that independent claims 1 and 5 are in condition for allowance and that the dependent claims, which depend directly or indirectly from independent claims 1 and 5, are also allowable for at least the same reasons, as well as for the additional limitations provided by these claims. Accordingly, all claims are in condition for allowance, and withdrawal is requested of the rejections under 35 U.S.C. §102(b) and §103(a).

CONCLUSION

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. It is believed that a full and complete response has been made to the outstanding Office Action, and that the present application is in condition for allowance.

However, if there are any outstanding issues, the Examiner is invited to telephone Sam Bhattacharya (Reg. No. 48,107) at 703-205-8000 in an effort to expedite prosecution.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,
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